ABSTRACT OF THE DISCLOSURE

A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns. Each of the non-volatile memory devices has: a word gate formed above a semiconductor layer with a gate insulating layer interposed; an impurity layer formed in the semiconductor layer; and control gates in the form of side walls formed along both side surfaces of the word gate. Each of the control gates consists of a first control gate and a second control gate adjacent to each other; the first control gate is formed on a first insulating layer which is a stack of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film; and the second control gate is formed on a second insulating layer formed of a silicon oxide film.